Amendments to the Claims

Claims 1-52 (Cancelled).

53. (Currently amended) A DRAM forming method comprising:

forming a first gate stack and a second gate stack over a substrate, each gate stack comprising a pair of opposing sidewalls;

defining a first, second, third and fourth diffusion regions within the substrate;

defining an isolation region between the first gate stack and the second gate stack, the isolation region electrically isolating the first and second gate stacks from each other;

forming a pair of spacers along opposing sidewalls of each gate stack; the first and second diffusion regions extending an initial distance under the spacers associated with the first gate stack, and the third and fourth diffusion regions extending an initial distance under the spacers associated with the second gate stack; ~~and~~

extending the first diffusion region relative to the initial distance without extending the second diffusion region, the extending comprising implanting a heavy p-type dopant; and

extending the fourth diffusion region relative to the initial distance without extending the third diffusion region.

54. (Canceled).

55. (Original) The method of claim 53 wherein the spacers comprise a spacer width and wherein the initial distance is less than the spacer width.

56. (Original) The method of claim 53 wherein each of the diffusion regions are conductively doped with a first type dopant and wherein the extending comprises halo implanting a second type dopant.

57. (Original) The method of claim 53 wherein the diffusion regions are majority doped with n-type dopant and wherein the extending comprises forming extension regions majority doped with p-type dopant.

58. (Original) The method of claim 53 wherein the isolation region comprises a shallow trench isolation region.

59. (Previously presented) The method of claim 53 further comprising:

forming a first and second capacitor constructions; the first capacitor construction being in electrical connection with the second diffusion region, and the second capacitor construction being in electrical connection with the third diffusion region; and

forming a first bit line contact in electrical connection with the first diffusion region and a second bit line contact in electrical connection with the third diffusion region.

60. (Original) The method of claim 53 wherein the defining an isolation region comprises:

forming a doped pocket region within the semiconductor substrate, the doped pocket region comprising a pocket width; and

forming an isolation mass over the substrate and over the pocket region, the isolation mass having a total mass width that is greater than the pocket width.

61. (Original) The method of claim 60 wherein the isolation mass comprises:

a gate stack over the substrate, the gate stack having opposing sidewalls;

a pair of insulative spacers along the opposing sidewalls, the total mass width being a distance between outer edges of the pair of insulative spacers measured at a surface of the substrate; and

wherein the total mass width is at least about double the pocket width.

Claims 62-64 (Cancelled).